BECKMAN/SDS

INTEGRATED COMPUTING SYSTEMS

HYBRID COMPUTATION: A GROWING NEED

THE NEED for simulating extremely complex scientific and engineering problems continues to grow. However, the high accuracy and dynamic ranges of these problems combined with real-time simulation requirements are beyond the practical capabilities of either an analog or scientific digital computer alone. This situation has created a demand for a hybrid computer which combines the benefits of both analog and digital computers.

In a hybrid system the analog computer can provide the high parallel operating speeds for real-time simulations, convenient means for mathematical modeling, and ease in varying parameters; the digital computer can provide the advantages of excellent resolution, precise arithmetic capabilities for numerical integration, complex control logic, and large storage capacities.

Properly designed, a hybrid computer offers the most efficient means for simulating problems such as these:

- Sampled data or computer-controlled systems simulations requiring the combination of continuous and discrete variables or data.
- Systems of differential equations to be solved at very high speed for prediction or optimization.
- Systems with transport delays.
- Simulation studies involving systems with both high and low frequency characteristics.
- Systems requiring on-line, real-time statistical analysis, data filtering, smoothing, and editing.
- Systems described by very large simultaneous sets of ordinary differential equations.

THE DEMAND for solving such problems has brought about the introduction of several so-called hybrid computers. These machines are usually linked by expensive, custom-designed equipment which only provide the basic communication between the analog computer and digital computer. The ability to produce effective software for programming such equipment becomes extremely difficult and economically impractical.

THE REQUIREMENTS for efficient hybrid computation can best be met by a computer system with standard, integrated hardware and software. The all-important linkage or interface equipment must insure optimum flow of data and control information between the analog computer and the digital computer. And perhaps most important, the software must simplify programming and enable the user to easily determine the most effective use of harware—without requiring an intimate knowledge of the hardware involved.

THE SOLUTION: BECKMAN / SDS INTEGRATED COMPUTING SYSTEMS

Beckman Instruments, Inc., and Scientific Data Systems have combined their broad experiences in analog and digital computation to offer you the first standard series of hybrid computers available. Unlike other so-called hybrid systems, Beckman/SDS computers are truly integrated computing systems—from hardware to software. State-of-the-art design concepts allow you to choose from six standard, all solid-state systems to meet your particular requirements.

With built-in expansion capabilities in both hardware and software, your Beckman/SDS Integrated Computing System can be economically expanded to satisfy your growing computational needs.

And to assure you of complete service, Beckman provides total systems responsibilities from initial assessment of your integrated computer requirements through installation and field service after delivery.

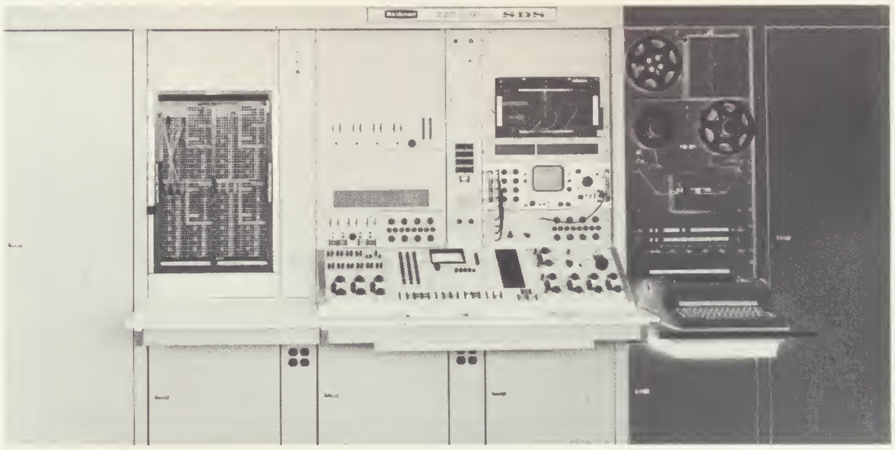
ANALOG SUBSYSTEM: THE NEW BECKMAN 2200 SERIES

The Beckman/SDS Integrated Computing Systems incorporate the most advanced analog subsystem available—the Beckman 2200 Series general-purpose analog computer. This totally new and completely solid-state analog computer was specifically designed for integrated operation.

All solid-state linear and nonlinear equipment is designed to insure exceptional static and dynamic performance characteristics. Only one basic type of amplifier is used throughout the system, minimizing spare parts and service requirements. Dither-free sine-cosine generators provide full rate resolution capabilities. Function generators are offered either in compact, easily accessible manual-set units or digitally controlled types which can be rapidly set by the digital subsystem. In addition you have the choice of either high-speed solid-state or reed-relay switching, or a combination of both types.

The fully shielded analog patchboard has a 3,600-terminal capacity and is organized for the most efficient use of the analog computing elements. The all-new program control board provides you with extremely flexible transference control of various computing elements and computing modes. You can quickly change an operational amplifier from a summer to an integrator or high-gain amplifier without disturbing the analog patchboard. The program control board also provides access to logic circuits such as gates and relay drivers.

To satisfy the most complex computations, patchable digital logic is available as an option. Flip-flops, electronic switches, function relays, and comparators permit you to quickly modify a control function, such as two different operating cycles or change parameters.



TYPICAL FULLY EXPANDED ANALOG SUBSYSTEM

Total Amplifier Complement	392*
Integrator-Summer-High Gain	72†
Summer-High Gains	48†
Summers (Used for DFG's and Multipliers)	32
Inverters	
Diode Function Generators	32
Multipliers	96
Sin-Cos and Rate Resolver System	112
Potentiometers (Phase Compensated)	
2 Terminal (Digitally Set)	240
3 Terminal (Manually Set)	24
Spare Resistor Networks (4 Inputs Each)	60
Electronic Multipliers (Digital or Quarter Square)	48
Electronic Sin-Cos and Rate Resolvers (Includes 4 Multipliers per channel not included in above 48 Multipliers)	8
Diode Function Generators	32
Function Switches	24
Comparator Amplifiers (Logic Output)	48
Function Relays	32
Electronic Switches	48
Noise Generator	1
Diode Limiters	
Feedbacks	32
Bridge Limiters (Off Board)	As Desired
Analog Patchboard	3600 Terminals
T-Trunks (To External)	240
P-Trunks (To Program Control Board)	16
Unassigned Trunks	80
Program Control Board Digital Logic Elements	
Schmitt/One-shots	4
RST Flip-flops	8
Inverters	8
Relay Drivers	16
Three-diode Networks	2
Logic Gates (3 Input)	6
Logic Gates (2 Input)	12
Electronic Switch Drive Lines	24
Comparator Outputs	24
Two-decade Preset Counters	4
Program Control Board	1196 Terminals
Q-Trunks (To External)	52
P-Trunks (To Analog Patchboard)	16
Unassigned	48
Patchable Digital Logic Module (Optional)	
Three-input Logic Gates	48
Schmitt/One-shots	8
Three-diode Networks	16
RST Flip-flops	16
Inverters	16
Four-bit Shift Registers	4
Status Lamp Drivers	
Assigned (Flip-flops, Comparators, Shift Registers)	56
Unassigned	16
Comparator Outputs	24
Electronic Switch Drive Lines	24
Two-decade Preset Counters	4
Logic Patchboard	1196 Terminals
Trunks to External	52
Trunks to Program Control Board	52
Unassigned	87

*Quarter Square Multipliers include two amplifiers per channel. For Digital or Quarter Square Multipliers with 3 amplifiers per channel, total is increased to 440 amplifiers.

†Integrator and Summer-High Gain analog patchboard layouts are identical. Additional Summer-High Gain Amplifiers can be installed initially and then expanded to Integrators in the field (up to 72).

INTERFACE SUBSYSTEM

The interface subsystem provides the two major paths of communication between the computer subsystems: the data channels and the control linkage. The data channels provide analog inputs and outputs to and from the digital subsystem, permitting the digital subsystem to exchange data and perform calculations on analog data and vice versa. The control linkage allows digital control of analog operations and communicates "sense" and "interrupt" information (originating in the analog) to the digital subsystem.

The digital subsystem with its arthimetic and decision-making capabilities performs hardware validations, calculates, sets up, and checks initial conditions. During computation it controls modes and may even alter the problem configuration while calculating and introducing new problem parameters as needed. In addition, data channels and control linkage can be used for communication with physical models, such as cockpit simulators.

DATA CHANNELS

DIGITAL-TO-ANALOG DATA CHANELS

Fourteen-bit (plus sign) data words from the digital subsystem converted into ±100-volt analog signals are available on the analog problem board for insertion in analog problem loops. Flip-flop registers associated with each DAC can be independently up-dated as determined by the digital subsystem program. For simultaneous up-dating of all DAC's, an additional level of storage is available as an optional feature.

ANALOG-TO-DIGITAL DATA CHANNELS

Data channels on the analog problem board are multiplexed into an analog-to-digital converter. The ADC converts the varying analog signals (100 VFS) into 14-bit (plus sign) digital words.

A track and hold amplifier associated with the ADC eliminates errors due to changes in the analog signals during digitizing. For simultaneous data transfer, track and hold amplifiers on each multiplexer input are available as an option. Through the digital subsystem program the multiplexer can be randomly addressed or sequentially stepped. Combined random-sequential stepping and high-speed single-channel operation can also be used.

CONTROL LINKAGE

POTSET AND READBACK

Through the point selection capability in the analog subsystem, a data word from the digital subsystem can be used to select and read back through the ADC any

STANDARD HYBRID SOFTWARE PACKAGES

MODEL 2200/92H **With 4K to 32K Memory** SYMBOLIC ASSEMBLER UTILITY PROGRAMS	**MODEL 2200/900H Series** **With Basic 4K Memory** UTILITY PROGRAMS HYBRID FORTRAN II HYBRID SYMBOL	**MODELS 2200/910H, 920H, 925H** **With 8K to 16K Memory*** UTILITY PROGRAMS HYBRID FORTRAN II HYBRID SYMBOL HYBRID EXECUTIVE HYBRID META SYMBOL
MODEL 2200/930H **With 8K to 32K Memory*** UTILITY PROGRAMS HYBRID FORTRAN II HYBRID SYMBOL HYBRID EXECUTIVE HYBRID META SYMBOL	**MODEL 2200/9300H** **With Basic 4K Memory** UTILITY PROGRAMS HYBRID FORTRAN II HYBRID SYMBOL	**MODEL 2200/9300H** **With 16K to 32K Memory*** UTILITY PROGRAMS HYBRID FORTRAN II HYBRID SYMBOL HYBRID EXECUTIVE HYBRID META SYMBOL HYBRID FORTRAN IV

*With SDS MAGPAK and Card Reader

DIGITAL SUBSYSTEM SELECTION CHART*

DIGITAL SUBSYSTEM	92H	910H	920H	925H	930H	9300H
WORD LENGTH	12-bit	24-bit				
CORE MEMORY, MAXIMUM	32,000	16,000			32,000	
MEMORY CYCLE TIME	1.75 μsec	8 μsec		1.75 μsec		
EXECUTION TIME						
FIXED POINT						
Add	3.5 μsec	16 μsec		3.5 μsec		1.75 μsec
Multiply	285 μsec†	248 μsec	32 μsec	54.25 μsec	7.0 μsec	
FLOATING POINT††						
Add		832 μsec	368 μsec	196 μsec	83 μsec	14 μsec
Multiply		1696 μsec	600 μsec	371 μsec	138 μsec	12.25 μsec

†Optional 7.0 μsec Multiply Instruction. ††39-bit fraction, 9-bit exponent.

*SDS H-Series Digital Computers, including full Hybrid Software Packages, are available only in Beckman/SDS Integrated Computing Systems.

of up to 10,000 points in the analog subsystem. Included are amplifiers, potentiometers, multipliers, function generators, and other computing elements. An unloading amplifier is used so that high impedance outputs such as potentiometers can be read.

The digitally set reference divider, in conjunction with the above selection and readback capabilities, allows the digital subsystem to set potentiometers, read back the set value and compare it against the desired setting.

SIGNAL AND SENSE LINES

An important benefit of the control linkage is the ability of the digital subsystem to communicate discrete commands to the analog subsystem and to sense the state of logic elements in the analog subsystem.

The signal-line outputs are both wired directly to perform control of the analog subsystem, and are available on the logic patchboard of the analog subsystem. The direct-wired signal lines are used to switch the analog subsystem through its states such as standby, initial condition, compute, and hold. Signal lines terminated on the logic patchboard allow you the flexibility of patching them to perform special control, depending upon the individual problem requirements. In conjunction with patchable logic elements, such as flip-flops and relay drivers, they may be used to switch problem configuration and variables, and change scaling.

The sense lines give the digital subsystem the capability of making decisions based on information from the analog subsystem. They also allow the digital subsystem to check that operations are being performed as commanded.

INTERRUPT LINES

Interrupts allow the occurrence of events in the analog subsystem to modify the digital subsystem program. Outputs such as overloads and analog comparator outputs can be programmed to interrupt the computer, allowing it to take action such as changing analog problem scaling.

INTERFACE FEATURES

Transformer coupling of all data and control lines provides complete isolation of analog and digital grounds.

ANALOG INPUT CHANNELS (ADC):	16 standard, 128 maximum.
SYSTEM INPUT RATE:	25,000 samples per second.
ANALOG OUTPUT CHANNELS (DAC):	8 standard, 128 maximum.
SYSTEM OUTPUT RATE:	190,000 words per second maximum.
SENSE LINES:	16 standard (expandable).
SIGNAL LINES:	16 standard (expandable).
PRIORITY INTERRUPTS:	16 standard (expandable).

DIGITAL SUBSYSTEMS: THE SDS 92H, 900H SERIES & 9300H

The Beckman/SDS Integrated Computing Systems are available with any one of six SDS H-Series digital computers. Complete, standard hybrid software packages are supplied with all H-Series digital subsystems—*at no extra cost.*

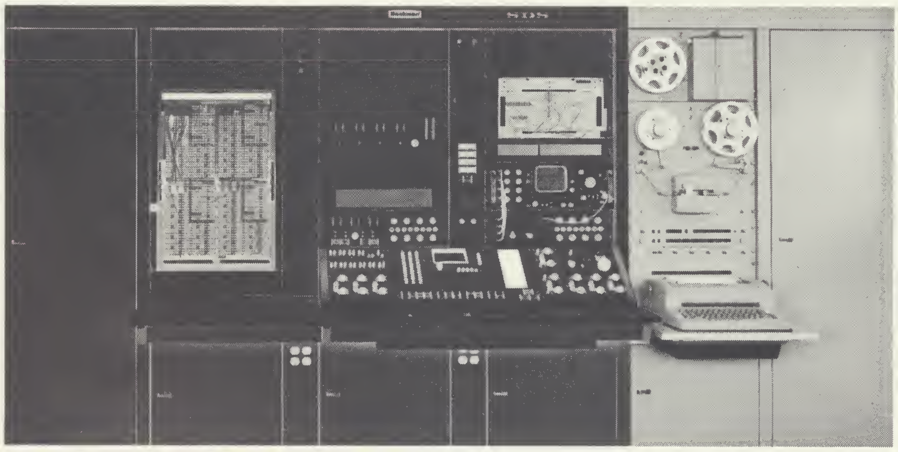
The SDS 92H provides real-time systems control, direct digital control, message switching, formatting and peripheral processing, and high-speed computation.

Input/output is compatible with that of SDS 900H Series computers so that the complete line of field-proven 900H Series peripheral equipment—including SDS MAGPAK—can be used without modification. And, like the SDS 900H Series computers, the 92H uses all-silicon seminconductors. Advanced SDS logic design techniques result in the use of from two to five times fewer components than conventionally designed equipment. This gives the SDS 92H a significant reliability advantage over comparable computers.

The SDS 900H Series digital subsystems provide more answers at lower cost and with greater reliability than any other general-purpose digital computers on the market today. The SDS 910H, 920H, 925H, and 930H are a family of compatible computers designed for scientific and engineering computation and for real-time systems integration. High internal computing speeds, powerful instruction lists, and a large number of efficient input/output systems insure maximum speed and flexibility for a wide variety of applications.

Each of these 900H Series computers meets a different range of requirements, but all four are compatible logically, electrically, and mechanically. Programs written for any 900H Series computer can be run on any other computer in the series. All 900H Series peripheral equipment can be used without modification on all four machines.

In the SDS 9300H, special attention has been given to features which facilitate integrating a computer into a real-time system. These include speed, flexible I/O, low component count for reliability, wide environmental tolerance, and small size. Real-time clocks, A-to-D converters, and displays are available as standard peripheral equipment.



AVAILABLE NOW: THE FIRST STANDARD HYBRID SOFTWARE*

Beckman/SDS offers you the first standard software packages specifically developed for hybrid computation. With all Beckman/SDS Integrated Computing Systems—regardless of size—you are furnished a complete standard library of hybrid software—and at no extra cost. You are not burdened by the time-consuming task and high cost of developing specialized programs for your specific or varying applications.

Beckman/SDS software packages consist of comprehensive programs which assure you of the most efficient man/machine communication. You concentrate on your simulation problems—not on the hardware. Programs are incorporated in a flexible easy to use system which simplifies and speeds the total programming process from set-up and checkout to actual computation and analysis. In addition programs consisting of maintenance and diagnostic routines are provided to insure minimum down-time and optimum performance of your integrated computing system.

The following descriptions are only a few of the program packages in the complete library of hybrid software available to you—today. And because of the continuing software development by Beckman/SDS, you are assured of an up-to-date, ever growing library—all free of charge.

HYBRID FORTRAN II

The HYBRID FORTRAN II language is problem-oriented as opposed to machine-oriented. This allows you to concentrate on the problem to be solved rather than the details of hardware operation. Expressions are used that are quite similar to accepted mathemetical notation involving the operational relationships of constants, variables, and function. Special instructions to the computer, such as input or output commands and data specifications, use names or mnemonics easily associated with corresponding English terms.

The HYBRID FORTRAN II processor takes programs written in the HYBRID FORTRAN II language and produces or compiles machine-language programs for execution on a Beckman/SDS Integrated Computing System. To minimize the cost of compiling—a major expense of today's computing installations—HYBRID FORTRAN II emphasizes compiling speed. In addition, features are included for use at run-time to reduce the cost and time required for program checkout and execution.

The most significant achievement in HYBRID FORTRAN II is not apparent in the language structure but is a feature of the compiler itself. This feature is the ability to have recurrsive interrupt-controlled subroutines. Normal FORTRAN II routines are not written to permit recurrsive interrupt and re-entry. These deficiencies are overcome by "pushdown" lists for both subordinate temporary storage and return address. Each time the subroutine is entered a flag is set to indicate the subroutine is in use and the temporary storage is saved in the LIST. In addition to restoring the digital state of the subroutines, the mode state of the analog subsystem must be restored after the interrup is serviced. This is accomplished in HYBRID FORTRAN II by maintaining a mode map in the digital subsystem. This mode map is used to remember the mode state.

To optimize run-time, some of the subroutines can be coded in SYMBOL. But the convenience of FORTRAN is available to save programming expense.

HYBRID SYMBOL

The HYBRID SYMBOL allows you to use the full capabilities of the Beckman/SDS Integrated Computing Systems, yet relieves you of the burdensome bookkeeping details inherent in machine-language programming. All operation codes, transfer location, and addresses are written in symbolic notation. A set of special pseudo operations simplifies the entry of constants and provides control information for the assembler. In addition, an extensive set of extended operations facilitates input/output operations and testing of various computer conditions.

HYBRID SYMBOL is a two-pass system which requires two readings of the source program for a complete assembly. Input can be from paper tape, cards, magnetic tape, or typewriter keyboard.

The first assembly pass assigns an absolute address to each symbol used in the location field of an instruction and stores the resulting entry in a symbol table. The second assembly pass replaces each operation mnemonic by the appropriate numeric code and substitutes the correct absolute address for any symbolic expression used in the variable field of the instruction. The entire instruction, including any indirect addressing and/or tagging, is assembled during the second pass and punched out, along with the appropriate control words, in the format specified by the user.

UTILITY PROGRAMS

A comprehensive library of UTILITY PROGRAMS is provided to insure you of efficient, economical use of the Beckman/SDS Integrated Computing System. These programs provide the benefits of ease of use, reduction of programming time, and automatic operation.

This software library includes analytic function subroutines such as sine, arcosine, exponential, and square root. Among the extensive list of problem analysis programs are Function Generation, Time Delay, and Anacheck (static checkout of the analog subsystem).

Matrix Package

A Matrix Package provides a set of subroutines for performing arithmetic operations on matrices of arbitrary size and configuration. In addition, subroutines permit the moving of arrays from one section of memory to another and enable you to locate any element in a matrix with a minimum of programming effort.

Help Utility System

The HELP program is a machine-language utility system designed to aid the machine-language programmer in the loading, debugging, and output of his programs.

Request Package

A special feature of the Beckman/SDS Integrated Computing System is the Request Package. The last portion of core memory storage is allocated to a special program which allows you convenient access to the analog subsystem via the input/output typewriters.

This program permits a wide choice of monitor and control functions all of which can be controlled from the typewriter keyboard.

The Request Package is a man-machine communication, and therefore a low priority entered via a low priority interrupt. If while the Request Package is being serviced a higher priority interrup occurs, the program will be shifted to the higher priority program. Upon completion of A-to-D and D-to-A conversions the program control will be returned to the Request Package. This use of priority interrupts allows you to use the Request Package without disturbing the main program.

Maintenance and Diagnostic Programs

Each Beckman/SDS Integrated Computing System is provided with a set of programs designed to facilitate maintenance and pinpoint equipment malfunctions. These programs are tailored to meet the specific requirements of the equipment configuration involved. The programs are used during scheduled maintenance periods to insure that all elements are functional and operating within prescribed tolerances. These programs also can be used to speed the diagnosis and repair of system malfunctions.

*SDS H-Series Digital Computers, including full Hybrid Software Packages, are available only in Beckman/SDS Integrated Computing Systems.

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NEW DEVELOPMENT IN HYBRID COMPUTATION

The October 10 issue of Business Week carried the announcement of the first Hybrid Computer being readied for delivery to the National Aeronautics and Space Administration.

In case you missed this important development, the facing page carries a reprint of our announcement. If you would like more details please call or write, today, to Beckman Computer Operations, 2200 Wright Avenue, Richmond, California, (94804), Telephone (415) 526-7730.

BECKMAN/SDS INTEGRATED COMPUTING SYSTEMS

Beckman Instruments, Inc., and Scientific Data Systems can now provide you with totally integrated computing systems. The combined skills and experience of each company's analog and digital technologies make this program possible. Various computer configurations allow you to choose a system that best suits your particular requirements.

Unprecedented capability is provided by:

- 8 different computers from standard product lines
- Continuing software development programs
- Computational facility for research and training
- Independent analog and digital operation

BECKMAN/SDS MODEL 2220/920

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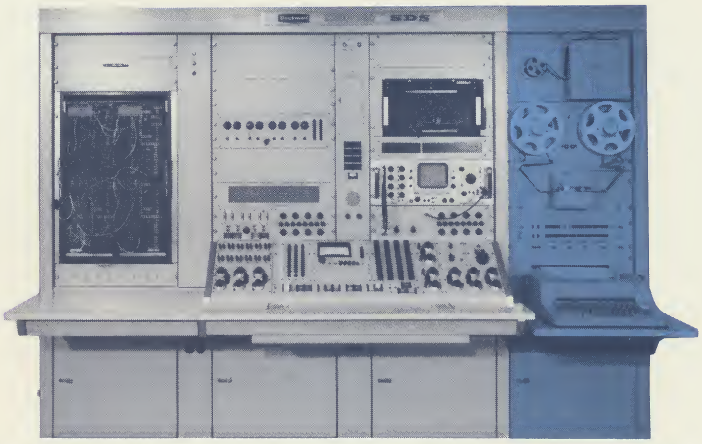
ANALOG THE NEW BECKMAN 2200 SERIES



Beckman 2200 Series general purpose analog computers incorporate advanced design techniques to provide these significant benefits:

- All solid state design, (±100 volts)
- Solid-state switching and/or reed relay mode control
- Standardized card size and mounting modules for all linear and non-linear equipment
- Compact design:
  - Fully expanded 2220 is only 2 cabinets plus console (Approx 10 feet total length).
  - Fully expanded 2230 is only 3 cabinets plus console (Approx 14 feet total length).
- New computing elements with improved performance
- New control structure, offering greater programming power and flexibility with improved Pinboard control system
- Control system and patchable logic prewired and designated for integrated system operation.

MODEL 2220 & 2230 SPECIFICATIONS

The 2200 Series computers are available in two expandable systems, each similar except for control console and computing capacity. Described below are the two basic computer systems.

2220	LINEAR	2230
48	Integrator-Summer-High Gain	72
24	Summer-High Gain	48
12	Summer (Used for DFG's and Multipliers)	24
52	Inverter (Used for DFG's and Multipliers)	96
	Potentiometers (Phase compensated)	
140	2 Terminal (Servo Set)	240
12	3 Terminal (Manual Set)	24
4	2 Terminal (Manual Set)	4
36	Spare Resistor Networks (4 inputs each)	60

2220	NON-LINEAR	2230
40	Electronic Multiplier	72
4	Electronic Sin-Cos and Rate Resolvers	6
	(Includes 4 of above Multipliers per channel)	6
12	Diode Function Generators	24
24	Function Switches	32
	Comparator Amplifiers	
8	Relay Output	16
4	Logic Output	8
1	Noise Generator	1
12	Dual Shunt Limiters	24
As Desired	Diode Bridge Networks (Off board components)	As Desired

2220	PATCHABLE LOGIC MODULE	2230
48	OR/NOR	48
16	Comparators	16
16	Electronic Switches	16
16	RST Flip-Flops	16
4	Shift Registers (4 Bits)	4
8	1 Shot	8
16	Inverters	16
4	Two Decade Counters	4
16	Relay Drivers	16
16	Operational Relay Coil Lines	16
44	Control Line (Analog logic busses)	44
100	T Trunks (Patchboard to External Connector)	200
16	P Trunks (Patchboard to Pinboard)	32
40	E Trunks (Pinboard to Patchable Logic)	40
52	Q Trunks (Patchable Logic to External Connectors)	52
	Unassigned Terminals:	
72	Patchboard	90
266	Pinboard	40
30	Logicboard	30
1012 holes	Pinboard/Pinbay Control System	1012 holes
2128 holes	Shielded Patchboard/Patchbay System	3600 holes
1196 holes	Logic Patchboard/Patchbay System	1196 holes

THE INTERFACE

The two major paths of communication between the computers are the data channels and the control interface. The data channels provide analog inputs and outputs to and from the digital computer, permitting the digital computer to exchange data and perform calculations on analog data and vice versa.

The control interface allows digital control of analog operations and communicates "sense" and "interrupt" information (originating in the analog) to the digital. The digital computer, with its arithmetic and decision making capability, performs hardware validations, calculates, sets up, and checks initial conditions. During computation it controls modes and may even alter the problem configuration while calculating and introducing new problem parameters as needed.

DATA INTERFACE

Digital-To-Analog Data Channels

Fourteen bit (signed) data words from the digital computer converted into ±100v analog signals, are available on the problem board for insertion in analog problem loops. Flip-flop registers associated with each DAC may be independently up-dated as determined by the digital computer program. Wherever simultaneous up-dating of all DAC's is required, an additional level of storage may be added.

Analog-To-Digital Data Channels

Data channels on the analog problem board are multiplexed into an analog-to-digital converter. The ADC converts the varying analog signals (100 V.F.S.) into 14 bit (signed) digital words.

A track and hold amplifier associated with the ADC eliminates errors due to changes in the analog signals during digitizing. For simultaneous data transfer, track and hold amplifiers on each multiplexer input are available as an optional feature. Through the digital computer program the multiplexer may be randomly addressed or sequentially stepped. Combined random-sequential stepping and high speed single channel operation may also be used.

CONTROL INTERFACE

Potset And Readback

Through the point selection capability in the analog computer, a data word from the digital computer may be used to select and read back through the ADC any of up to 10,000 points in the analog computer. Included are amplifiers, potentiometers, multipliers, function generators and other computing elements. An unloading amplifier is used so that high impedance outputs such as potentiometers can be read.

The digitally set reference divider, in conjunction with the above selection and readback capability, allows the digital computer to set potentiometers, read back the set value, and compare it against the desired setting.

Signal And Sense Lines

An important strength of the control interface is the ability of the digital computer to supply discrete commands to the analog computer and to sense the state of logic elements in the analog computer.

The signal line outputs are available on the logic patchboard of the analog computer. This allows the operator the flexibility of patching them to perform special control depending upon the individual problem requirements. The signal lines may be used directly to switch the analog computer through its states such as standby, initial condition, compute, hold, iterative computation, etc. In conjunction with patchable elements, such as flip-flops and relay drivers, they may be used to switch problem configuration and variables, change scaling, etc.

The sense lines give the digital computer the capability of making decisions based on information from the analog computer. This also allows the digital computer to check that operations are being performed as commanded.

Interrupt Lines

Interrupts allow the occurrence of events in the analog computer to modify the digital computer program. Outputs such as overloads, analog comparator outputs, etc., can be programmed to interrupt the computer, allowing it to take action, such as changing analog problem scaling.

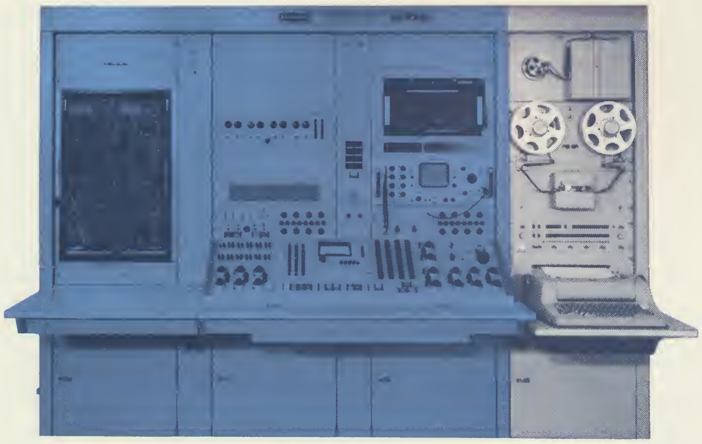
INTERFACE FEATURES

Transformer coupling of all data and control lines, for complete isolation of analog and digital grounds.

Analog Input Channels (ADC):	8 standard, 128 maximum
System Input Rate:	25,000 samples per second
Analog Output Channels (DAC):	8 standard, 128 maximum
System Output Rate:	300,000 words per second maximum
Sense Lines:	16 standard—expandable to 2048
Signal Lines:	16 standard—expandable to 204
Priority Interrupts:	16 standard—expandable to 896

Analog and digital input and output channels to outside world for communication with physical modules, cockpit simulators, etc. These also permit use of the digital subsystem as a full-capability, high accuracy data collection/processing system.

DIGITAL THE SDS 900 & 9000 SERIES



All SDS 900 & 9000 Series digital computers offer you the following features:

- High speed, low cost, general purpose operation
- 24-bit word plus parity bit
- Binary arithmetic
- Up to 1024 priority interrupts
- Parity check of all memory and input/output operations
- Multi-level indexing and indirect addressing
- All-silicon semiconductors
- A wide variety of peripheral equipment including:
  - Paper Tape I/O equipment
  - High and low speed Card Readers and Punches
  - High and low speed Line Printers
  - Multi-density, high and low speed Magnetic Tape Units (IBM-compatible)
  - Magnetic Drum Memory Units
  - Magnetic Disc Memory Units
  - Display Equipment
  - SDS Magpak Magnetic Tape System

SDS 910

- Basic core memory 2,048 words, expandable to 16,384 words, all directly addressable
- Typical execution times (including memory access **and** indexing)
  - Add .... 16 μsec
  - Multiply .... 248 μsec
  - Floating Point Operations
    - (24-bit Fraction plus 9-bit Exponent)
      - Add .... 440 μsec
      - Multiply .... 504 μsec
    - (39-bit Fraction plus 9-bit Exponent)
      - Add .... 832 μsec
      - Multiply .... 1696 μsec

SDS 920

- Basic core memory 4,096 words, expandable to 16,384 words, all directly addressable
- Typical execution times (including memory access **and** indexing)
  - Add .... 16 μsec
  - Multiply .... 32 μsec
  - Floating Point Operations
    - (24-bit Fraction plus 9-bit Exponent)
      - Add .... 292 μsec
      - Multiply .... 248 μsec
    - (39-bit Fraction plus 9-bit Exponent)
      - Add .... 368 μsec
      - Multiply .... 600 μsec

SDS 930

- Basic core memory of 4,096 words expandable to 32,768 words, all addressable
- Up to 8 buffered I/O channels with rates 2 million character per second
- Typical execution times (including memory access **and** indexing)
  - Fixed-Point Operations
    - Add .... 3.85 μsec
    - Multiply .... 7.7 μsec
    - Divide .... 19.25 μsec
  - Floating-Point Operations
    - (24-bit fraction plus 9-bit exponent)
      - Add .... 81 μsec
      - Multiply .... 59 μsec
    - (39-bit fraction plus 9-bit exponent)
      - Add .... 91 μsec
      - Multiply .... 152 μsec

SDS 9300

- Basic core memory of 4,096 words, expandable to 32,768 words, all directly addressable
- 48-bit word for floating-point arithmetic
- 3 Index Registers and Indirect Addressing with unlimited address cascading
- FORTRAN II and IV, a Symbolic Assembler, and a Monitor System as part of a complete software package
- 11 high-speed search operations operate at 1.75 μseconds per item
- Eight automatic data channels that operate upon words or characters, each capable of fully buffered operation at one word every 1.75 μsecond, simultaneously with computation
- Execution times, including all accesses and indexing (using overlapped memories):
  - Fixed-Point
    - Add .... 1.75 μsec
    - Double Precision Add .... 3.5 μsec
    - Multiply .... 7.0 μsec
    - Shift (24 positions) .... 5.25 μsec
  - Floating-Point
    - (39-bit fraction, 9-bit exponent)
      - Add .... 14.0 μsec
      - Multiply .... 12.25 μsec
  - Extensive repertoire of more than 110 instructions

THE NEED FOR AN INTEGRATED COMPUTING SYSTEM

Many of the computing demands created by today's advanced problems are beyond the capabilities of analog computers or incompatible with the structure of digital machines. This growing class of problems, outside the scope of either machine alone, is increasing the demand for a hybrid computer system which takes advantage of the great resolution, storage, arithmetic and control capabilities of digital computers, and the parallel operating speed, ease of modeling, and ease of parameter variation found in analog computers.

The following classes of problems are all likely candidates for efficient solution on this type of integrated computing system:

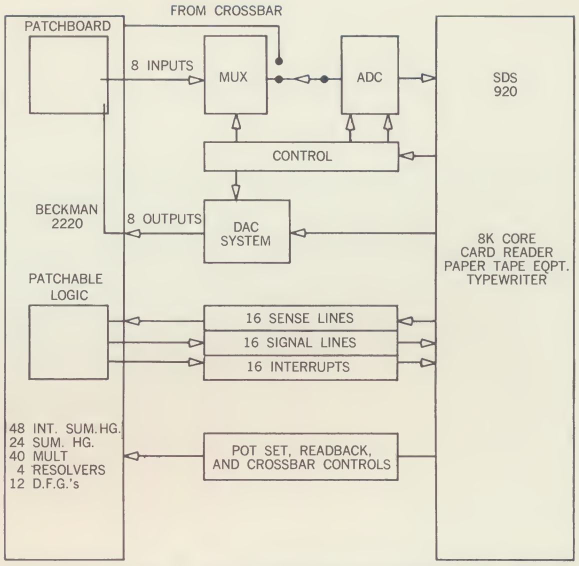
- Simulation studies involving systems having both high and low frequency characteristics
- Systems of differential equations which are to be solved at very high speed for prediction or optimization studies
- Sampled data or computer-controlled systems simulations requiring the combination of continuous and discrete variables or data
- Systems with transport delays
- Systems requiring on line, real-time statistical analysis, data filtering, smoothing, editing, etc.
- Systems described by very large simultaneous sets of ordinary differential equations

SPECIAL ADVANTAGES

Beckman/SDS supplies, with its systems, a complete set of operating computer programs to insure optimal performance during every phase of operation. Also, a computation facility, in Santa Monica, California, is staffed and maintained by Beckman and SDS to provide you with a tool for properly assessing the integrated computing system which will best suit your needs. The facility also serves as a research and training center for integrated computation.

Comprehensive two week courses in hybrid computation are offered at the Beckman/SDS Computation Center. This insures adequate training of your systems analysists and provides them with actual experience in solving problems on an integrated computing system. The number of attendees is limited to 16 people per course in order to insure individual attention to each student.

The end result is a Beckman/SDS integrated computing system with capability, flexibility and growth potential . . . for both your present and future simulation and analysis requirements.



CONFIGURATION OF THE INTEGRATED COMPUTING SYSTEM MODEL 2220/920

PROGRAMMING THE INTEGRATED COMPUTING SYSTEMS

Beckman Instruments and Scientific Data Systems provide a specialized programming system that insures the efficient and economic use of their integrated analog-digital computing systems. This user-oriented programming package—software—minimizes the cost and effort of day-to-day operation by providing programmed aids.

These programs are incorporated into a flexible, easy to use operating system that simplifies and speeds the total programming process from analysis through set up and check-out to actual computation and results. The programming package allows all of these functions to be carried out in an automatic fashion. Thus, the user enjoys the benefits of ease of use, reduction of programming time, automatic operation and complete documentation. Because of the continuing software development and maintenance effort by Beckman/SDS, the user is assured of an up-to-date, ever growing library of routines designed specifically for hybrid computing systems.

Beckman® INSTRUMENTS, INC.

COMPUTER OPERATIONS

RICHMOND, CALIFORNIA • 94804

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A Parallel/Sequential, Stored-Program Hybrid Signal Processor

by JOSEPH D. GRANDINE and THOMAS G. HAGAN

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by JOSEPH D. GRANDINE and THOMAS G. HAGAN, *Adage, Inc.,* Cambridge, Massachusetts

INTRODUCTION

The analog versus digital debate gave way several years ago to more fruitful examination of various hybrid systems in which analog and digital techniques are combined. The complementary nature of the strengths and weaknesses of analog and digital approaches has inspired a number of different hybrid systems aimed at combining the separate advantages of the analog and digital disciplines. The strength of the analog approach is its speed, realized through use of multiple arithmetic operators functioning in parallel. Digital techniques offer opportunity for storage, logical control, and for arithmetic operations carried out to much higher precision than the .01% possible with analog techniques.

Most hybrid systems built to date have contained as major elements complete analog or digital computers which had originally been designed for use as independent computing systems. In fact, the inclusion of an analog or digital computer serves as a useful basis for classifying hybrid systems. In such a taxonomy, hybrid systems of one class are those formed by linking together an analog computer and a digital computer. Much of the present enthusiasm for hybrid computers stems from successful experience of the past several years with hybrid computing systems of this type.

A second type of hybrid is achieved by starting with a conventional analog computer and adding digital elements. Almost all analog computers now manufactured are in fact hybrids of this type since they include, in greater or lesser degree, patchable digital elements to implement various logic and control functions.

A third class of hybrid system is formed by adding analog elements to a conventional digital computer. The added analog elements provide, in effect, an extension of the arithmetic unit contained within the digital computer. Successful systems of this type have been built at the Electronic Systems Laboratory at MIT, and have demonstrated that the processing capability of the digital computer can be very significantly increased with a relatively small amount of analog hardware.

Three types of hybrids are thus possible in which an analog computer, a digital computer, or both, are included in the hybrid system. Each of these approaches has been used successfully to realize some of the potential advantages of hybrid computing.

A fourth type of hybrid is that which contains neither an analog nor a digital computer, but is instead built up from more basic analog and digital elements. This class of hybrid permits a more fundamental approach to design and organization of the system. Compared to those hybrids in which major segments of the system were originally designed for separate existence as independent analog or digital computers, it is possible to achieve a closer integration of analog and digital techniques. The designer has more freedom to optimize allocation of tasks to analog and digital elements, and to seek the best balance between parallel and sequential operation.

The subject of this paper is a hybrid data system designed with these goals in mind—the AMBILOG 200 Stored Program Signal Processor shown in Figure 1.

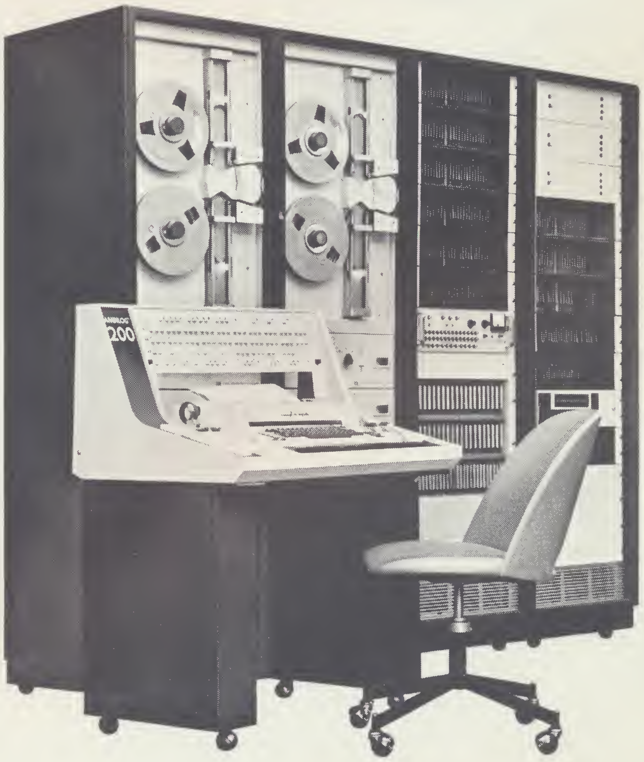

Figure 1—AMBILOG 200 Stored Program Signal Processor

SYSTEM ORGANIZATION

Inputs and outputs of the AMBILOG 200 are both analog and digital in nature; the system organization is shown in Figure 2. Analog signal paths are shown as double black lines; digital signal paths are shown as single lines. The system provides multiple input/output channels for both analog and digital signals.

The system resembles a digital computer in that it functions by executing, in sequential fashion, a program stored in core memory. Activities of the user in programming and operating the system resemble the activities associated with programming and operating a digital computer. One prepares a program by writing down a sequence of instructions; the program is entered manually via switches at the console or through the typewriter; or one may prepare, off-line, a punched paper tape which can then be carried to the machine, inserted into a paper tape reader, and loaded into core storage. The AMBILOG 200 has in common with digital computers, therefore, the logical power and programming convenience of stored-program operation. It differs from digital computers in these respects:

a. Many arithmetic operations are carried out by analog and hybrid analog/digital ("ambilogical") elements.

b. Multiple arithmetic operators are used in parallel.

c. The instruction repertoire is especially organized to facilitate data transfers among, and control of, this array of parallel operators.

d. Extensive analog input/output is provided, under direct program control.

e. The priority interrupt system is structured to permit an unusual degree of responsiveness to events occurring asynchronously in the external world.

The hybrid arithmetic section includes a parallel array of analog and hybrid elements used for performing arithmetic operations, comparisons, high-speed analog/digital and digital/analog conversion, and routing of analog signals under digital control. Operation of the system is controlled by instructions executed sequentially by the system control unit. The system control unit alternately fetches and executes instructions. Instructions executed by the system control unit accomplish high-speed transfer of data and control words to and from registers contained in the hybrid arithmetic section, core memory, and various digital input/output devices such as I/O typewriter, tape reader, tape punch, and digital magnetic tape units.

Instructions are fetched either from the core memory system or from an external instruction bus. A priority interrupt system determines where each instruction is to come from and gates one of many external instruction sources into the external instruction bus. In the absence of a service request from a priority interrupt channel associated with an external instruction source, instructions come from core memory.

The core memory subsystem provides storage of values, control words, and instructions. Each memory location stores 30 bits which may represent:

a. Two 15-bit single precision data values.
b. One 30-bit double-precision data value.
c. One 30-bit control word.
d. One 30-bit instruction.
e. Five 6-bit characters.

The basic memory cycle is two microseconds. Memory sizes range from 1,024 words to 32,768 words.

Analog signals in the system represent numerical values with $+20V = +1.000$ and $-20V = -1.000$. Digital signals represent binary numbers between $+1.000$ and -1.000, with ONE'S complement notation for negative numbers. The system interprets both single-precision sign-and-14-bit digital values, and double-precision sign-and-29-bit values. Hybrid arithmetic is carried out with operands represented both by analog signals and single-precision (15-bit) digital data values. A 30-bit digital accumulator operating upon double-precision 30-bit operands augments the hybrid arithmetic.

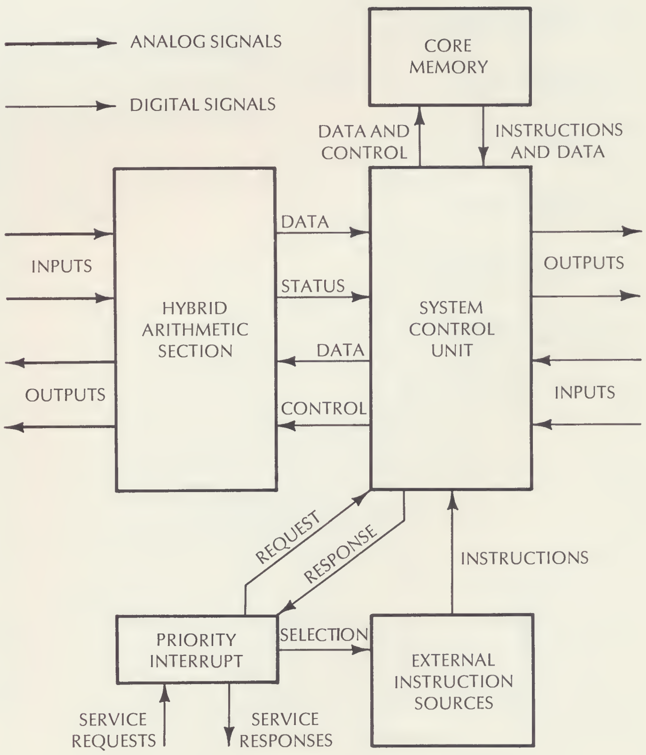

Figure 2 — System Organization

HYBRID SUBSYSTEMS

Hybrid devices are used in the AMBILOG 200 for signal steering, summing, multiplying, and dividing. Routing of analog signals is performed by digitally controlled analog switches. Summing operations are accomplished by high-speed precision operational amplifiers. Multiplication and division are implemented as truly hybrid operations, with an analog signal multiplied or divided by a digital signal to produce an analog result.

Signal steering, summing, multiplication, and division functions are all accomplished by a hybrid subsystem called the ACE (ambilogical computing element). A functional diagram of the ACE is shown in Figure 3. The ACE has six analog inputs, a digital data input and a digital control input. The output is an analog signal.

Seven control bits specify the function performed by the ACE. Six bits are used for selecting the analog inputs to be steered to a summing amplifier. Any combination of the six analog inputs may be selected for summing. The result of the selection and summing operation is an analog signal which is applied to a hybrid multiplier/divider. The seventh control bit selects either multiplication or division. The 15-bit digital data input is comprised of sign and 14-bits for value. Multiplication and division are implemented with solid-state switches and precision resistors assembled into precision, digitally-controlled analog attenuators. In the ACE, two such attenuators are used — one as the input resistor and one as the feedback resistor for the output operational amplifier. Conductance of the attenuator is directly proportional to the 14-bit parallel digital data input to the attenuator. Selection of multiplication or division operation is accomplished by digitally gating the 14-bit ACE value input either to the input attenuator or the feedback attenuator. For operation as a multiplier, the 14-bit digital input is gated to the input attenuator, while the feedback attenuator is made equal to unity. For division, the input attenuator is made equal to unity, and the digital data word is steered to the feedback attenuator.

The ACE functions as a full four-quadrant device, with positive and negative polarities allowed for both analog and digital inputs. The analog output assumes the polarity appropriate to the result of the computation. Four-quadrant performance is implemented by switching an inverter into the path of the signal between the summing selector and the multiplier/divider, according to the algebraic sign of the digital data input.

The ACE provides a one-bit overflow output which is "true" whenever the output exceeds full scale. Such overflow can occur, for example, when attempting to divide by too small a number.

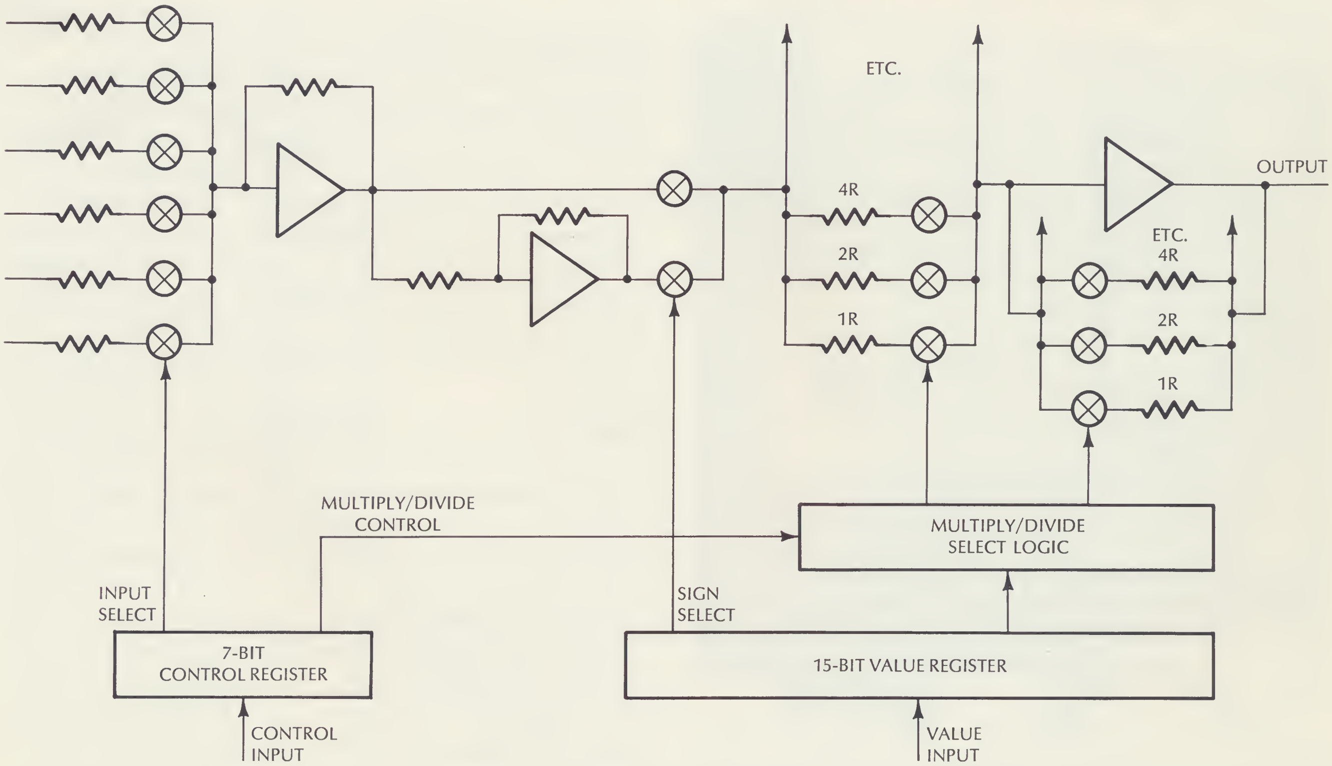

Figure 3 — Functional Diagram of the ACE

Other hybrid subsystems used in the AMBILOG 200 are shown in Figure 4. The analog signal multiplexer (AMX) selects a single input channel corresponding to a digital channel number and steers that analog signal to its output terminal. The sample-and-hold amplifier (SAH) operates in a sample or hold mode in response to a one-bit digital control signal. In the sample mode, the analog output tracks the analog input. In the hold mode, the output holds at the value prevailing at the time of transition from sample to hold. The digital-to-analog converter (DAC) converts a single precision 15-bit digital value into the corresponding analog signal. The analog-to-digital converter (ADC) converts an analog signal into the corresponding single-precision digital value in response to a one-bit digital control signal. Over-range indication is provided as a one-bit digital output.

The comparator (CMP) subsystem contains an internal DAC whose analog output is presented along with six other analog input signals to a summing selector. Any combination of these seven may be selected and summed to produce an analog output. A 7-bit control register specifies the analog signals selected for summing. Outputs provided are an analog signal equal to the selected sum, and a one-bit digital output representing the sign of the selected sum. The comparator subsystem permits high-speed comparison between a digital data value and the sum of selected analog signals.

The hybrid subsystems in the AMBILOG 200 have these features in common:

a. Analog signals internal to the machine are $\pm 20V$ full scale.

b. Full four-quadrant operation (all combinations of signs of inputs and outputs are permitted).

c. Each analog output can drive up to 10 analog inputs.

d. Analog output of any subsystem is accurate to within .01% of full scale within 10 microseconds following any change of inputs. When individual subsystems are connected in series, the array has a settling time which increases approximately as the square root of the number of subsystems in series.

e. With some exceptions, digital registers for data and control inputs and outputs are contained within the subsystems themselves.

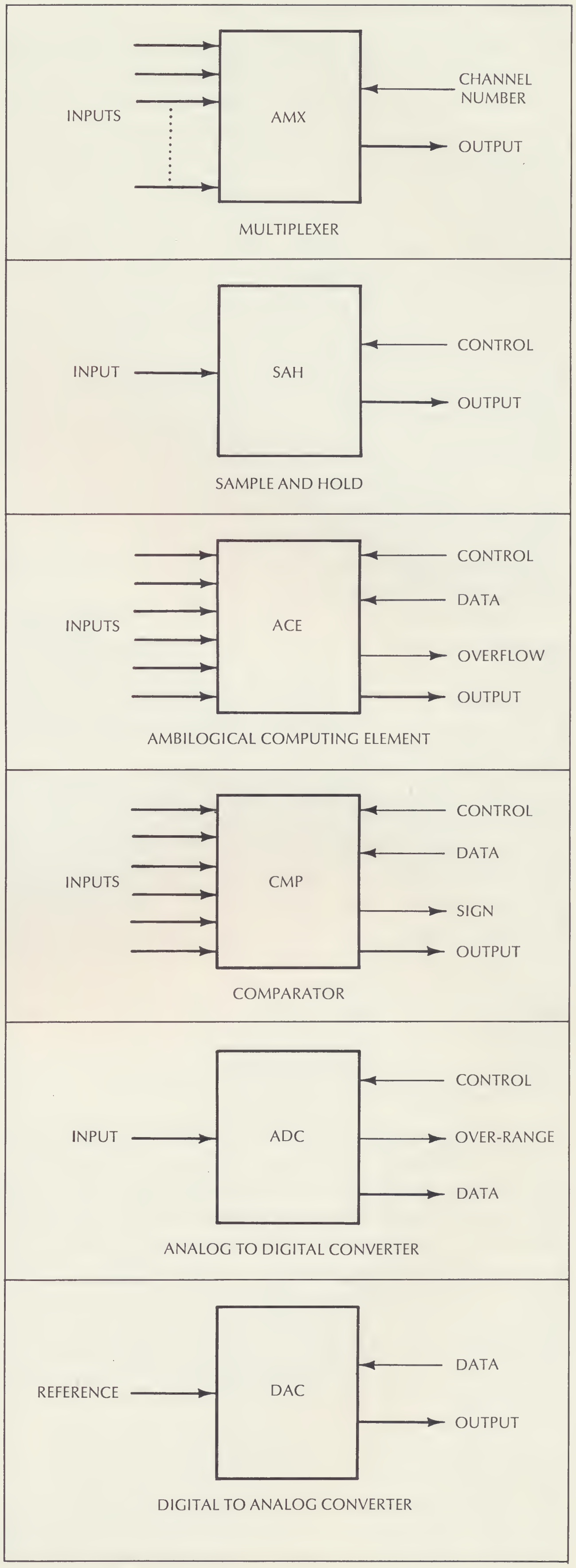

Figure 4 — Hybrid ("Ambilogical") Subsystems Used in the AMBILOG 200

PARALLEL HYBRID ARITHMETIC

The hybrid operators described above are assembled into an array somewhat resembling that of a conventional analog computer. Within the array, hybrid operators all function in parallel and operate simultaneously upon multiple analog and digital operands. Different combinations of subsystems can be assembled and wired into a variety of hardware configurations. Signal routing within such a hardware configuration is determined not by patch panel interconnections, but by programmatic control of the selection switches incorporated in the subsystems. All the useful interconnections among approximately a dozen hybrid subsystems can be accomplished under program control without recourse to patch panels. An array of six or a dozen elements, small compared to the assemblages of fifty to several hundred operators common in analog computers, provides substantial computing performance because it can be operated in high-speed sequential or iterative fashion under close stored-program control.

A typical hardware configuration of hybrid subsystems is shown in Figure 5. This configuration operates upon analog inputs *X*, *Y* and *Z*, and digital inputs *A*, *B*, *C*, *D*, *E*, *F* and *G*, to produce the result, *R*, in analog form, and, by passing it through the *ADC*, in digital form.

A very large number of relationships among the various analog and digital operands presented as inputs to this configuration can be evaluated. The particular arithmetic relationship evaluated is determined by the states of the various control-bit flip-flops in the ACE's and the comparator. All the control flip-flops located in the ACE's and the comparator of this configuration can be loaded simultaneously from a single 30-bit parallel digital control word. It is this control word that determines the particular arithmetic expression evaluated by the arithmetic unit.

In essence, each control word transmitted to the hybrid arithmetic unit is an arithmetic instruction, requesting evaluation of the particular arithmetic expression signified by the control word. The hybrid arithmetic unit therefore can be thought of as implementing the execution of a large number of different arithmetic instructions, including the evaluation of relatively complex expressions which in conventional digital machines require sequential execution of a series of instructions. For example, the expression—

$$R = A + B(X + C) + D(Y + E) + (Z + G)/F$$

can be evaluated by transmitting the appropriate input control word to the arithmetic unit. This one operation produces a result relating three analog variables and seven digital operands, requiring six additions, two multiplications and one division. Examples of some of the many expressions that can be evaluated by the arithmetic unit of Figure 5 are tabulated in Figure 6.

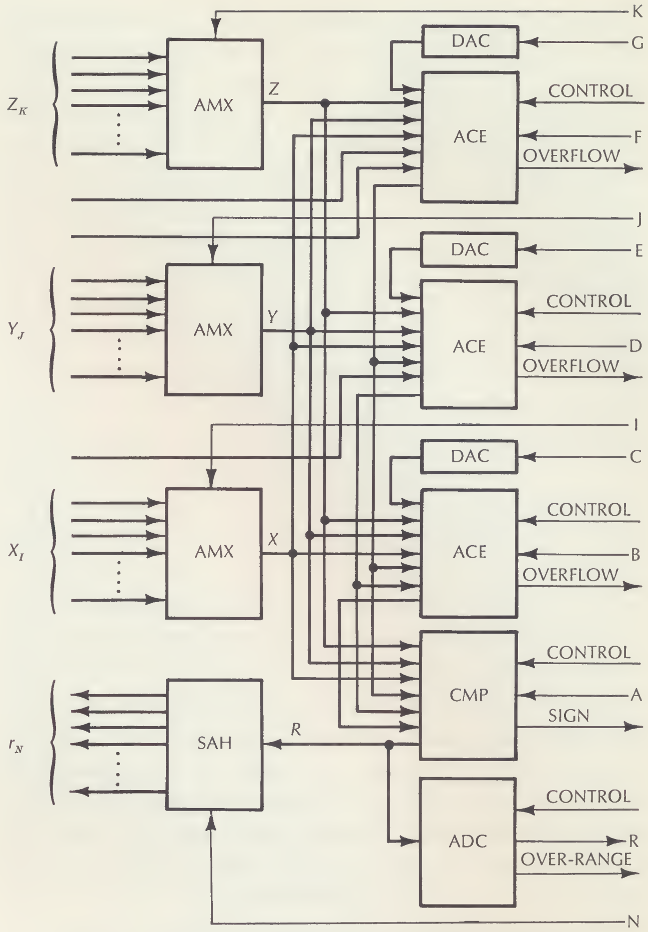

Figure 5 — Typical Configuration of Hybrid Subsystems

The hybrid arithmetic unit is utilized by moving appropriate digital operands into the various data registers, and then transmitting an expression-control word to the flip-flops comprising the control register. These steps result in the evaluation of *R* as an analog quantity. The result can be recovered as a digital quantity with one additional step to perform an analog-to-digital conversion.

$X + Y$	$\frac{GFD}{B}$
$X + Y + Z$	
$A + BX + DY + FZ$	$\frac{(Y + G)B}{FD}$
$A + B(X + C) + D(Y + E) + F(Z + G)$	
$BC + DE + FG$	$\frac{[(X + G)F + Y + E]D + C}{B} + A$
$GFDB + A + X$	
$A + GF + DGF + BDGF$	$\frac{G + X}{F} + \left[\frac{E + Y}{D} + Z + C\right]B$

Figure 6 — Some of the Expressions That Can Be Evaluated by the Configuration of Figure 5

DIGITAL DATA TRANSFER AND CONTROL

The primary role of the system control unit is the transfer of data and control words to and from core memory and back and forth among the digital registers incorporated in the various hybrid and digital subsystems and input/output devices. These data transfers are accomplished by transfer logic which provides a 30-bit wide data path for moving data from selected source to selected destination. Data transfers are accomplished one 30-bit word at a time. Execution of a transfer instruction permits transfer of a 30-bit control word, a 30-bit double-precision value, or two 15-bit single-precision values. Several logical operations can be accomplished in the course of transferring data from source to destination. Transfer operations are specified by an instruction held in the instruction register within the system control unit.

Function of the transfer system is shown in Figure 7. The transfer logic selects one of eight 30-bit data sources and one of sixteen 30-bit data destinations. As the data word is transferred, it may be rotated 0, 1, 6, or 15 bits left. The rotated word can be copied into the selected destination; or it can be complemented and copied into the destination; or it can be OR'd with the contents of the destination; or it can be AND'd with the contents of the selected destination. Results of these operations replace the previous contents of the selected destination, with the source left unchanged, unless it was specified as both source and destination for the transfer.

The OR and AND functions provided by the transfer logic permit setting and resetting the individual bits in any destination register. This allows turning particular bits ON or OFF in a control register without disturbing the states of other bits in the register.

The instruction format has been designed to facilitate transfers of data and control words needed for effective use of the parallel operator arrays. A multifield format permits simultaneous selection of source and destination, control of memory, and specification of word rotation and Boolean logical operations. Provision is made for instruction modification through indirect addressing and indexing.

All conditional instructions, jumps, and skips use a special instruction format differing only slightly from the format used for normal transfer instructions. The two formats used for instructions are shown in Figure 8.

Normal transfer instructions serve to move operands and control words into the value and control registers of the hybrid subsystems from memory or other digital sources, and to move *ADC* results and status information from the hybrid section into memory or other destinations. Transfer instructions serve also for digital arithmetic: digital addition is accomplished by specifying the digital accumulator as the destination for a data transfer.

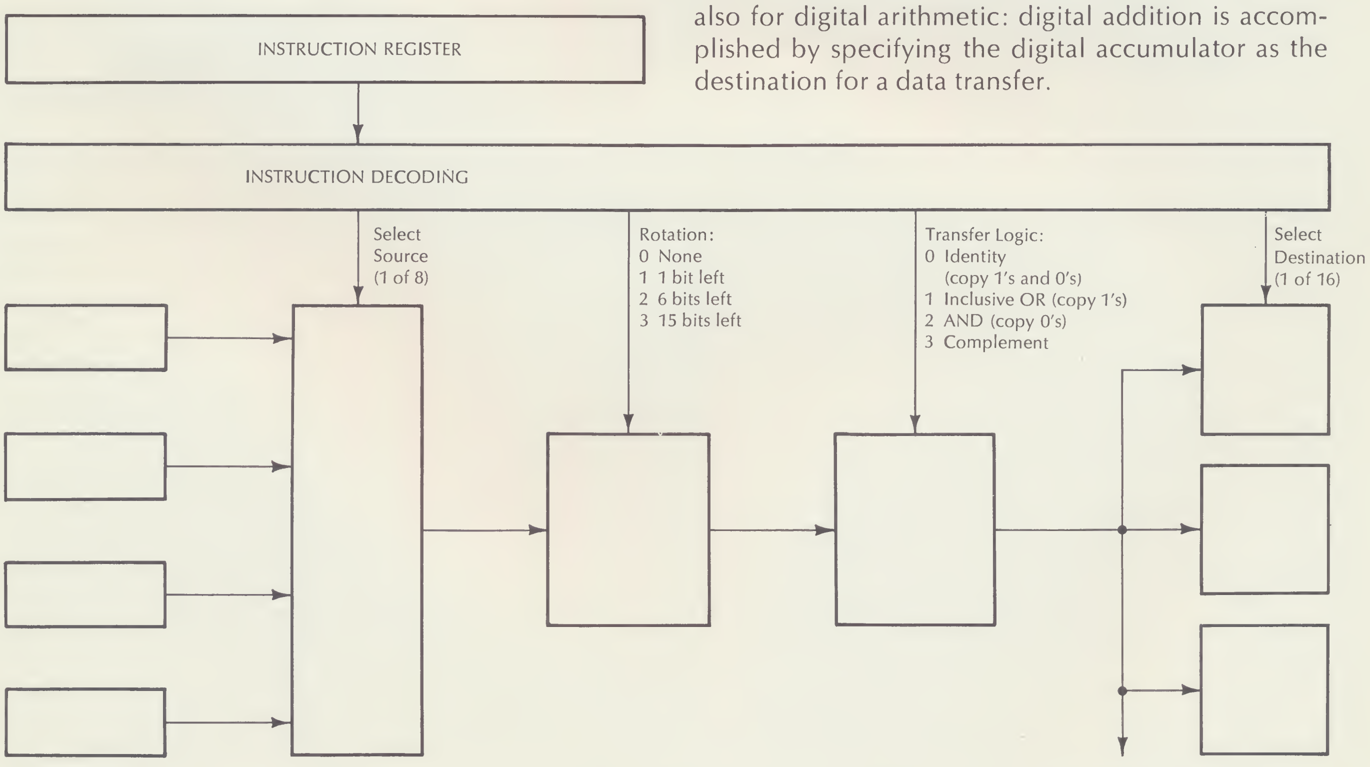

Figure 7 — Inter-Register Transfer Logic, From Selected Source to Selected Destination

NORMAL INSTRUCTION FORMAT (M = 1, 2, 3)

0 1	2 3 4 5	6 7 8	9 10	11 12	13	14
M Instruction Mode	D Destination	S Source	R Rotation	T Transfer Logic	X Index	I Indirect Address

15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
15 — A Address or Operand — 29

M = INSTRUCTION MODE
octal
- 0 Special Instruction
- 1 Random Memory Address
- 2 Sequential Memory Address
- 3 Immediate Execution (no memory cycle)

SPECIAL INSTRUCTION FORMAT (M = 0)

0 1	2 3 4 5	6 7 8 9 10	11 12	13	14
M = 0	D Destination	C Operation Code	T Transfer Logic	X Index	I Indirect Address

15 16 17 18 19 20 21 22 23 24 25 26 27 28 29
15 — A Address or Operand — 29

C = OPERATION CODE
octal
- 00 Generate Interrupt Request
- 01 JSR to A, (LC) $\rightarrow$ A, A + 1 $\rightarrow$ LC
- 02 JUMP to A, A $\rightarrow$ LC
- 03 If (AR) $<$ 0, JSR to A
- 04 If (AR) $<$ 0, JUMP to A
- 05 If (AR [15 — 29]) $\neq$ 0, JSR to A
- 06 If (AR [15 — 29]) $\neq$ 0, JUMP to A
- 07 If (AR) $<$ 0, SKIP Next Instruction, (LC) + 1 $\rightarrow$ LC
- 10 If (AR [15 — 29]) $\neq$ 0, SKIP
- 11 If A $\odot$ (S4[0 — 14]) $\neq$ 0, SKIP
- 12 If A $\odot$ (S4[15 — 29]) $\neq$ 0, SKIP
- 13 If (AR) $<$ 0, Transfer (A) to destination
- 14 If (AR[15 — 29]) $\neq$ 0, Transfer (A) to destination
- 15 . . . . 37 } Generate Interrupt Requests

Figure 8 — Instruction Format

APPLICATIONS

Stored-program hybrids of the type here described lend themselves to a variety of signal processing and simulation applications, especially to real-time problems requiring analog input or output.

Parallel/sequential system organization results, pleasantly and not unexpectedly, in the translation of problem statements into operating programs with far fewer instructions than are required by more highly sequential machines.

Listed below are several typical applications, along with the total number of instructions required for complete programs, including initialization, loop-closing and housekeeping operations:

a. Multichannel analog data acquisition, with arbitrary channel sampling sequence, conversion to engineering units, high- and low-limit test, formatting, and continuous magnetic tape output (105 instructions).

b. Generation of an arbitrary function of one variable by table look-up and cubic interpolation, with analog or digital input and analog or digital output (24 instructions).

c. Generation of an arbitrary function of two variables by table look-up and quadratic interpolation with cross-term; analog or digital inputs and output (38 instructions).

d. Measurement of time intervals between axis crossings of an analog input, and generation of a histogram showing frequency of occurrence versus length of interval (30 instructions).

e. Weighted Fourier transformation of multiple analog input signals, with arbitrary time-domain weighting function (57 instructions).

BECKMAN®/ INTEGRATED COMPUTING SYSTEMS

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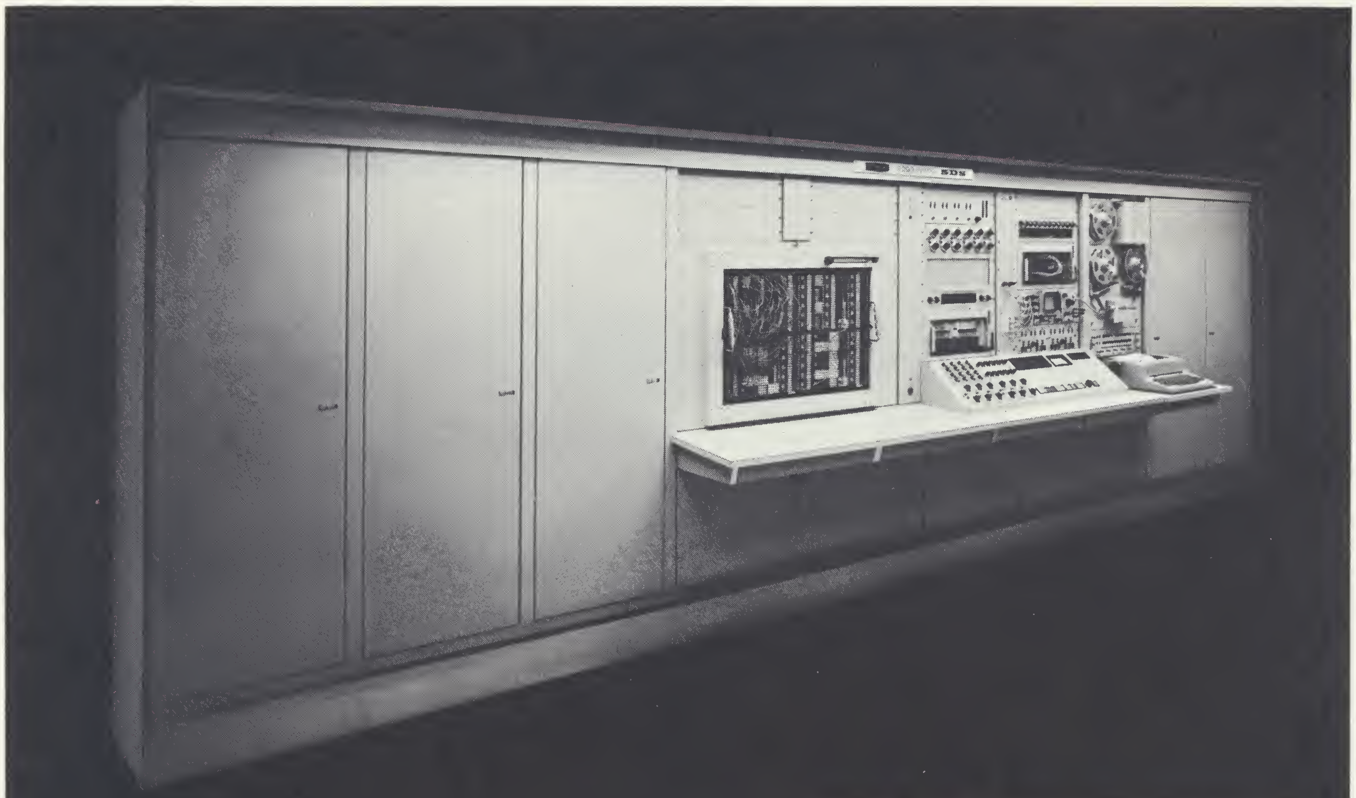
Problem Solving Power Through Total System Capability



The Beckman Model 2230 Integrated Computing System

THE BECKMAN APPROACH IN HYBRID COMPUTATION

The Beckman Integrated Computing System answers the demand! It offers you "problem solving power" through total system capability. Beckman accomplishes this through standard integrated hardware and software, developed by technological know-how that has long assured professional satisfaction within the industry.

HARDWARE

Beckman Instruments, Inc., and Scientific Data Systems, combining their broad experience in analog and digital computation, now offer you the first standard series of hybrid computers available. This allows you to choose from any six standard, all-solid-state systems to meet your particular needs. The all-important linkage or interface, which insures optimum flow of data and control information, is *standard*; therefore, there are no extra engineering or development costs.

SOFTWARE

Beckman hybrid software is designed to simplify programming and enable the user to easily determine the most effective use of the computer — without his acquiring an intimate knowledge of the hardware involved. Beckman offers you the first standard software packages specifically designed for hybrid computation. With all Beckman Integrated Computing Systems — regardless of size — you are furnished a complete *standard* library of hybrid software at no extra cost. And because of the continuing software development by Beckman, you are assured of an up-to-date, ever growing library — again at no extra cost!

PLUS:

A complete operational software package is delivered with each system. Hybrid compilers, assemblers, maintenance and diagnostic programs, as well as a complete library of mathematical and utility routines are provided at no cost.

The Beckman Computation Center offers new software developments, hybrid training courses, and application engineering assistance to all Beckman users.

With built-in expansion capabilities in both hardware and software, your Beckman integrated computing system can be economically expanded to satisfy your growing computational needs.

Beckman warranty and service, unequalled in the industry, provide total system responsibilities from your initial acquisition of a Beckman integrated computing system, through installation and field service after delivery. All the resources and reputation of Beckman Instruments, Inc., guarantee you our responsible performance.

ANALOG SUBSYSTEMS

The Beckman Integrated Computing Systems incorporate the most advanced analog subsystem available — the Beckman Model 2230 general-purpose analog computer. This totally new and completely solid-state analog computer was specifically designed for integrated operation.

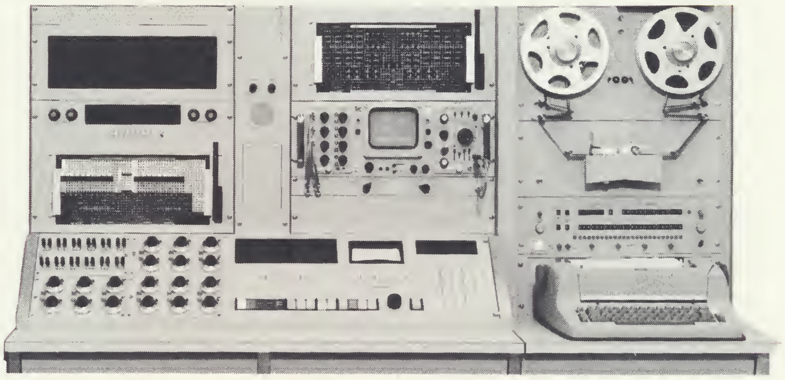
All solid-state linear and nonlinear equipment is designed to insure exceptional static and dynamic performance characteristics. Only one basic type of amplifier is used throughout the system, minimizing spare parts and service requirements. Dither-free sine-cosine generators provide full rate resolution capabilities. Function generators are offered either in compact, easily accessible manual-set units or digitally controlled types which can be rapidly set by the digital subsystem. In addition you have the choice of either, or both, solid-state and reed-relay switching.

CONSOLE

Through the use of newly designed patchboards, the analog and digital subsystem control console offers optimum flexibility and convenience for the operator. All controls are functionally grouped to simplify the operators command of the problem.

The use of the control patchboard eliminates the need for control wiring on the Analog Patchboard for use where they are needed; namely, the interconnection of problem voltages.

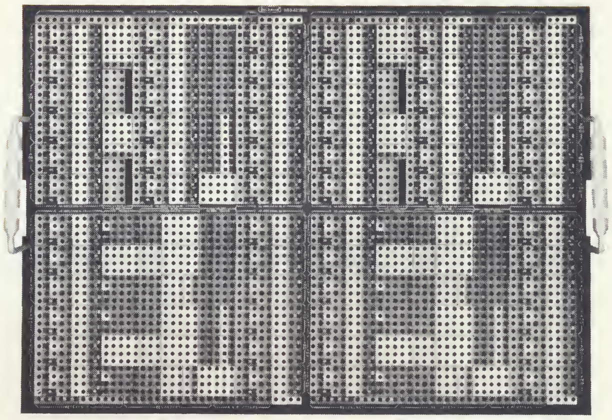
This design approach results in many additional advantages. The layout of the analog patchboard is not compromised by including control terminals. This results in an increase of up to 50% in linear equipment (amplifiers and potentiometers) available on the control console. A logic patchboard is available as an option.



ANALOG PATCHBOARD

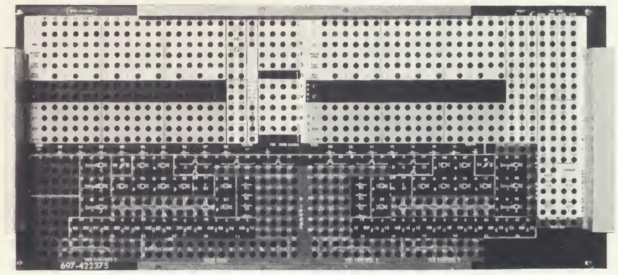
The fully shielded removable analog patchboard has a 3,600-terminal capacity and is organized for the most efficient use of the analog computing elements. The patchboard consists of four quadrants of diallyl phthalate, bonded to brass plates. The patchboards are constructed such that, when inserted in the patchboard, the cord shields contact the brass plate. This construction affords a shield over the entire patchboard against interference or electrical noise.

Entire problem signal interconnections are set up on the patchboard. These connections, to various components and functional component groups, are represented on the patchboard by blocks or designated areas of holes. Inputs, outputs, and control signals to functional components each have separate holes. When patching a mechanization, the output of one functional component is patched into an input of another functional group. Circuit configurations of individual components are established by patching within the appropriate block. Various terminals are color-coded in accordance with their individual connections, with various abbreviations describing function or ultimate connection of the terminal.



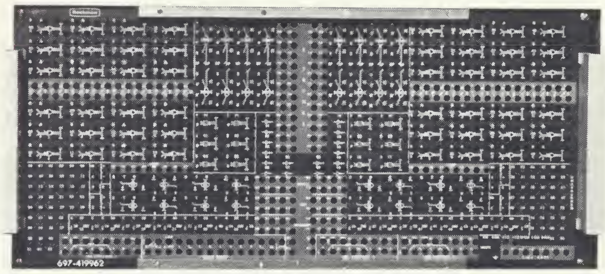
CONTROL PATCHBOARD

The control patchboard's basic function is to select the proper computer configuration required for a particular problem. It provides the means of controlling the circuits of the computing elements, such as hot-pinning/patching during the problem checkout phase, storage of the entire board for problem re-entry, and prepinning/patching for problem preparation independent of the computer. The control patchboard permits the operator to establish the type of computation required through transference selection, keeping all control wiring isolated from signal patching. (Analog Patchboard). You can quickly change an operational amplifier from a summer to integrator or high-gain amplifier without disturbing the analog patchboard. It also provides access to digital logic circuits located in the control patchbay. These digital circuits may be used in solving complex problems or whenever logic levels are desired.



LOGIC PATCHBOARD (OPTIONAL)

To satisfy the most complex computations, patchable digital logic is available as an option. Flip-flops, electronic switches, function relays, and comparators permit you to quickly modify a control function, such as two different operating cycles or change parameters. The quantity of the logic equipment in the system may be expanded at any time through the addition of this logic patchboard which provides greater problem flexibility.



INTERFACE SUBSYSTEM

The interface subsystem provides the two major paths of communication between the computer subsystems: the data channels and the control linkage. The data channels provide analog inputs and outputs to and from the digital subsystem, permitting the digital subsystem to exchange data and perform calculations on analog data and vice versa. The control linkage allows digital control of analog operations and communicates "sense" and "interrupt" information (originating in the analog) to the digital subsystem.

The digital subsystem with its arithmetic and decision-making capabilities performs hardware validations, calculations, sets up, and checks initial conditions. During computation it controls modes and may even alter the problem configuration while calculating and introducing new problem parameters as needed. In addition, data channels and control linkage can be used for communication with physical models, such as cockpit simulators.

DATA CHANNELS

DIGITAL-TO-ANALOG DATA CHANNELS

Fourteen-bit (plus sign) data words from the digital subsystem converted into ±100-volt analog signals are available on the analog problem board for insertion in analog problem loops. Flip-flop registers associated with each DAC can be independently up-dated as determined by the digital subsystem program. For simultaneous up-dating of all DAC's, an additional level of storage is available as an optional feature.

ANALOG-TO-DIGITAL DATA CHANNELS

Data channels on the analog problem board are multiplexed into an analog-to-digital converter. The ADC converts the varying analog signals (100 VFS) into 14-bit (plus sign) digital words.

A track and hold amplifier associated with the ADC eliminates errors due to changes in the analog signals during digitizing. For simultaneous data transfer, track and hold amplifiers on each multiplexer input are available as an option. Through the digital subsystem program the multiplexer can be randomly addressed or sequentially stepped. Combined random-sequential stepping and high-speed single-channel operation can also be used.

CONTROL LINKAGE

POTSET AND READBACK

Through the point selection capability in the analog subsystem, a data word from the digital subsystem can be used to select and read back through the ADC any of up to 10,000 points in the analog subsystem. Included are amplifiers, potentiometers, multipliers, function generators, and other computing elements. An unloading amplifier is used so that high impedance outputs such as potentiometers can be read.

The digitally set reference divider, in conjunction with the above selection and readback capabilities, allows the digital subsystem to set potentiometers, read back the set value and compare it against the desired setting.

SIGNAL AND SENSE LINES

An important benefit of the control linkage is the ability of the digital subsystem to communicate discrete commands to the analog subsystem and to sense the state of logic elements in the analog subsystem.

The signal-line outputs are both wired directly to perform control of the analog subsystem, and are available on the logic patchboard of the analog subsystem. The direct-wired signal lines are used to switch the analog subsystem through its states such as standby, initial condition, compute, and hold. Signal lines terminated on the logic patchboard allow you the flexibility of patching them to perform special control, depending upon the individual problem requirements. In conjunction with patchable logic elements, such as flip-flops and relay drivers, they may be used to switch problem configuration and variables, and change scaling.

The sense lines give the digital subsystem the capability of making decisions based on information from the analog subsystem. They also allow the digital subsystem to check that operations are being performed as commanded.

INTERRUPT LINES

Interrupts allow the occurrence of events in the analog subsystem to modify the digital subsystem program. Outputs such as overloads and analog comparator outputs can be programmed to interrupt the computer, allowing it to take action such as changing analog problem scaling.

INTERFACE FEATURES

Transformer coupling of all data and control lines provides complete isolation of analog and digital grounds.

ANALOG INPUT CHANNELS (ADC):	20 standard, expandable.
SYSTEM INPUT RATE:	25,000 samples per second.
ANALOG OUTPUT CHANNELS (DAC):	20 standard, expandable.
SYSTEM OUTPUT RATE:	190,000 words per second, max.
SENSE LINES:	16 standard, expandable.
SIGNAL LINES:	16 standard, expandable.
PRIORITY INTERRUPTS:	16 standard, expandable.

DIGITAL SUBSYSTEMS

Beckman Integrated Computing Systems are available with any one of six SDS H-Series digital computers.

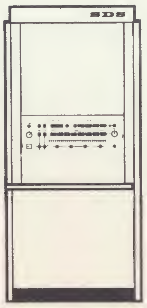
The SDS 92H provides real-time systems control, direct digital control, message switching, formatting and peripheral processing, and high-speed computation.

Input/output is compatible with that of SDS 900H Series computers so that the complete line of field-proven 900H Series peripheral equipment — including SDS MAGPAK — can be used without modification. And, like the SDS 900H Series computers, the 92H uses all-silicon semiconductors. Advanced SDS logic design techniques result in the use of from two to five times fewer components than conventionally designed equipment. This gives the SDS 92H a significant reliability advantage over comparable computers.

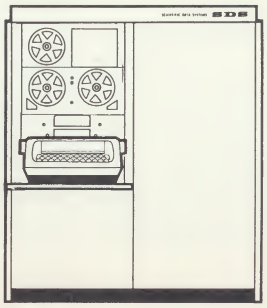
The SDS 910H, 920H, 925H, and 930H are a family of compatible computers designed for scientific and engineering computation and for real-time systems integration. High internal computing speeds, powerful instruction lists, and a large number of efficient input/output systems insure maximum speed and flexibility for a wide variety of applications.

Each of these 900H Series computers meets a different range of requirements, but all four are compatible logically, electrically, and mechanically. Programs written for any 900H Series computer can be run on any other computer in the series. All 900H Series peripheral equipment can be used without modification on all four machines.

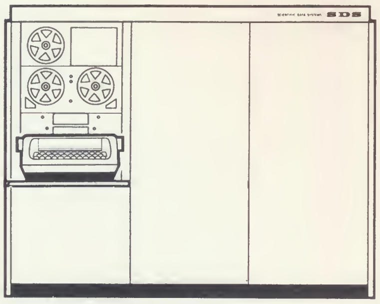
In the SDS 9300H, special attention has been given to features which facilitate integrating a computer into a real-time system. These include speed, flexible I/O, low component count for reliability, wide environmental tolerance, and small size. Real-time clocks, A-to-D converters, and displays are available as standard peripheral equipment.



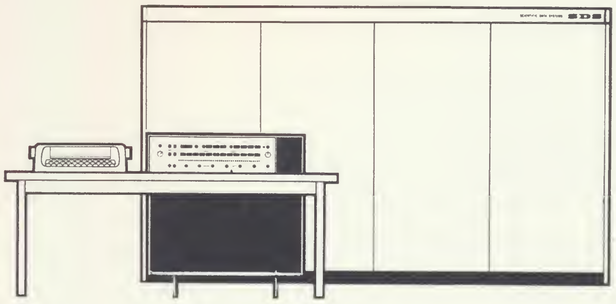
SDS 92H
Digital Subsystem



SDS 910H or SDS 920H
Digital Subsystems



SDS 925H or SDS 930H
Digital Subsystems



SDS 9300H Digital Subsystem

SPECIFICATIONS

TYPICAL FULLY EXPANDED ANALOG SUBSYSTEM

Total Amplifier Complement	392*
Integrator-Summer-High Gain	72†
Summer-High Gains	48†
Summers (Used for DFG's and Multipliers)	32
Inverters	
Diode Function Generators	32
Multipliers	96
Sin-Cos and Rate Resolver System	112
Potentiometers (Phase Compensated)	
2 Terminal (Digitally Set)	240
3 Terminal (Manually Set)	24
Spare Resistor Network (4 Inputs Each)	60
Electronic Multipliers (Digital or Quarter Square)	48
Electronic Sin-Cos and Rate Resolvers (Includes 4 Multipliers per channel not included in above 48 Multipliers)	8
Diode Function Generators	32
Function Switches	24
Comparator Amplifiers (Logic Output)	48
Function Relays	32
Electronic Switches	48
Noise Generator	1
Diode Limiters	
Feedbacks	32
Bridge Limiters (Off Board)	As Desired
Analog Patchboard	3600 Terminals
T-Trunks (To External)	240
P-Trunks (To Program Control Board)	16
Unassigned Trunks	80

Program Control Board Digital Logic Elements

Schmitt/One-shots	4
RST Flip-flops	8
Inverters	8
Relay Drivers	16
Three-diode Networks	2
Logic Gates (3 Input)	6
Logic Gates (2 Input)	12
Electronic Switch Drive Lines	24
Comparator Outputs	24
Two-decade Preset Counters	4
Program Control Board	1196 Terminals
Q-Trunks (To External)	52
P-Trunks (To Analog Patchboard)	16
Unassigned	48

Patchable Digital Logic Module (Optional)

Three-input Logic Gates	48
Schmitt/One-shots	8
Three-diode Networks	16
RST Flip-flops	16
Inverters	16
Four-bit Shift Registers	4
Status Lamp Drivers	
Assigned (Flip-flops, Comparators, Shift Registers)	56
Unassigned	16
Comparator Outputs	24
Electronic Switch Drive Lines	24
Two-decade Preset Counters	4
Logic Patchboard	1196 Terminals
Trunks to External	52
Trunks to Program Control Board	52
Unassigned	87

*Quarter Square Multipliers include two amplifiers per channel. For Digital or Quarter Square Multipliers with 3 amplifiers per channel, total is increased to 440 amplifiers.

†Integrator and Summer-High Gain analog patchboard layouts are identical. Additional Summer-High Gain Amplifiers can be installed initially and then expanded to Integrators in the field (up to 72).

DIGITAL SUBSYSTEM SELECTION CHART*

DIGITAL SUBSYSTEM	92H	910H	920H	925H	930H	9300H
WORD LENGTH	12-bit	24-bit				
CORE MEMORY, MAXIMUM	32,000	16,000			32,000	
MEMORY CYCLE TIME	1.75 μsec	8 μsec		1.75 μsec		
EXECUTION TIME FIXED POINT Add	3.5 μsec	16 μsec		3.5 μsec		1.75 μsec
Multiply	285 μsec†	248 μsec	32 μsec	54.25 μsec	7.0 μsec	
FLOATING POINT†† Add		832 μsec	368 μsec	196 μsec	83 μsec	14 μsec
Multiply		1696 μsec	600 μsec	371 μsec	138 μsec	12.25 μsec

†Optional 7.0 μsec Multiply Instruction. ††39-bit fraction, 9-bit exponent.

***SDS H-Series Digital Computers, including full Hybrid Software Packages, are available only in Beckman Integrated Computing Systems.**

STANDARD HYBRID SOFTWARE PACKAGES

MODEL 2230/92H
With 4K to 32K Memory
SYMBOLIC ASSEMBLER
UTILITY PROGRAMS

MODEL 2230/900H
With Basic 4K Memory
UTILITY PROGRAMS
HYBRID FORTRAN II

MODELS 2230/910H, 920H, 925H
With 8K to 16K Memory*
UTILITY PROGRAMS
HYBRID FORTRAN II
HYBRID EXECUTIVE

MODEL 2230/930H
With 8K to 32K Memory*
UTILITY PROGRAMS
HYBRID FORTRAN II
HYBRID EXECUTIVE

MODEL 2230/9300H
With Basic 4K Memory
UTILITY PROGRAMS
HYBRID FORTRAN II

MODEL 2230/9300H
With 16K to 32K Memory*
UTILITY PROGRAMS
HYBRID FORTRAN II
HYBRID EXECUTIVE
HYBRID FORTRAN IV

*SDS MAGPAK and Card Reader also available

For further information on Beckman Hybrid Software, utilize the attached reply card to receive your copy of brochure C065539, "BECKMAN / FIRST IN HYBRID SOFTWARE." This software brochure offers more detail on the aforementioned programs, plus a description of how Beckman offers greater system control through priority interrupt structure, independent programming, and recursive subroutines.

BECKMAN HYBRID SOFTWARE

Beckman offers you the first standard software packages specifically developed for hybrid computation. With all Beckman Integrated Computing Systems — regardless of size — you are furnished a complete standard library of hybrid software — and at NO EXTRA COST! You are not burdened by the time-consuming task and high cost of developing specialized programs for your specific or varying applications.

Beckman hybrid software can be classified into two general categories: Programming Systems and Utility Systems. A programming system such as an assembler or compiler simplifies the programmer's task in specifying a sequence of operations for solving his problem. The Utility Systems aid in specific tasks, such as a program for automatically performing a static check of the analog subsystem of a hybrid calculation.

PROGRAMMING SYSTEMS

HYBRID FORTRAN II

The Beckman hybrid computer, when incorporating either a 900 or 9000 Series SDS digital subsystem, utilizes Hybrid Fortran II. Special instructions to the computer, such as input or output commands and data specifications, use names or mnemonics easily associated with corresponding English terms. Expressions are used that are quite similar to accepted mathematical notations involving the operational relationships of constants, variables, and function.

As is the case with all Beckman hybrid programming systems, the generated code is completely compatible with interrupt operation. In the Hybrid Fortran II system many statements beyond the scope of normal Fortran are acceptable. These are listed below:

1. All ASA Fortran II standard definitions
2. Hybrid Fortran statements
   For example:
   Intra Computer Data Transfer
   Computer Set Up and Check Out
   Computer Mode Control
3. Logical Statements
   These follow the ASA Fortran IV definitions and include:
   AND, OR, NOT and Exclusive OR (EOR).
4. In-Line Symbol
   By placing an "S" in column one, the statement is interpreted as Symbol and one line of machine code is generated.
5. Interrupt Connections
   By use of the statements, Connect and Release, subroutines may be linked to and released from interrupt lines.

HYBRID FORTRAN IV

The HYBRID FORTRAN IV system, an extension of HYBRID FORTRAN II, allows you more flexibility in program implementation and features an improved language structure. The HYBRID FORTRAN IV compiler accepts a source program written in a language closely resembling ordinary mathematical notation. Designations such as complex variables and double-precision real-time variables eliminate the need for declaring the mode of a statement when writing the program. Also, decisions can be based on Boolean variables. Subroutines and functions may refer to storage arrays with dimensions, allowing flexibility in subprogram design and obviating recompilation to change dimension statements.

HYBRID EXECUTIVE

The HYBRID EXECUTIVE system automates the processing of intermixed programs, compilations, and executions with a minimum of operator intervention. The system utilizes magnetic tape units for recording of programming systems and utility systems.

UTILITY SYSTEMS

A comprehensive library of UTILITY PROGRAMS is provided to insure you of efficient, economical use of the Beckman Integrated Computing System. These programs provide the benefits of ease of use, reduction of programming time, and automatic operation.

ANACHECK

This Fortran coded program performs AUTOMATICALLY a static checkout of the analog subsystem against a specified analog flow chart listing. This automatic checkout eliminates the need for the operator's time-consuming supervision of problem verification. ANACHECK not only checks patchboard wiring and function of computing elements, but indicates if proper contact is being made on all connections . . . AUTOMATICALLY.

REQUEST PACKAGE

A special feature of the Beckman Integrated Computing System is the Request Package. The last portion of core memory storage is allocated to a special program which allows you convenient access to the analog subsystem via the input/output typewriters.

This program permits a wide choice of monitor and control functions all of which can be controlled from the typewriter keyboard.

MAINTENANCE AND DIAGNOSTIC PROGRAMS

Each Beckman Integrated Computing System is provided with a set of programs designed to facilitate maintenance and pinpoint equipment malfunctions. These programs are tailored to meet the specific requirements of the equipment configuration involved. The programs are used during scheduled maintenance periods to insure that all elements are functional and operating within prescribed tolerances. These programs also can be used to speed the diagnosis and repair of system malfunctions.

Digital Subsystem — The Examiner System is a complete diagnostic package designed to exercise and/or diagnose the memory, digital computer logic, buffer, and associated peripheral equipment.

The Examiner System is composed of the following programs:

1. Memory Diagnostics Program
2. Instruction Diagnostics Program
3. Peripheral Diagnostics Program

Analog Subsystem — The Analog Subsystem Diagnostics package is designed to utilize the digital subsystem for program control and type-out of individual component failure. Program design allows you to perform checks on the entire complement of analog equipment automatically, or to select individual components or groups of components.

The system is composed of five diagnostic subprograms: (1) Amplifier, (2) Servo-set Potentiometer, (3) Electronic Multipliers, (4) Sin-Cos Function Generator, and (5) Electronic Comparators and Patchable Logic.

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(415) 526-7730; TWX: 415-236-8933

INTERNATIONAL SUBSIDIARIES: GENEVA, SWITZERLAND; MUNICH, GERMANY; GLENROTHES, SCOTLAND; PARIS, FRANCE; TOKYO, JAPAN; CAPETOWN, SOUTH AFRICA

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- ☐ Beckman Analog Computers
- ☐ Beckman Software Brochure
- ☐ Your regular company mailing
- ☐ Have a Beckman Technical Representative call

This information required for:

- ☐ Immediate Procurement
- ☐ Future Procurement
- ☐ Reference Only
- ☐ A solution to my problem outlined below

Remarks ______________________________

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